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SOA-Based Optical Logic Circuit Development and Demonstration

DARPA/Army contract W911NF-06-1-0060
3/15/2006 to 6/14/2008

Final Report

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Massachusetts Institute of Technology
September 30, 2008

In this program, we investigated the fabrication and optical characterization of a photonic integrated circuit (PIC) designed for telecommunication applications using ultrafast (> 100Gbits/s) optical logic. The basic components in the PIC are active components, such as semiconductor optical amplifiers (SOAs), integrated with passive, light-routing waveguides. Optical switching is accomplished by embedding the amplifiers within the arms of Mach-Zehnder interferometers (MZIs), whereas power splitting of propagating signals is carried out within multimode interferometers (MMIs). Figure 1 shows a schematic of the basic unit cell under investigation.

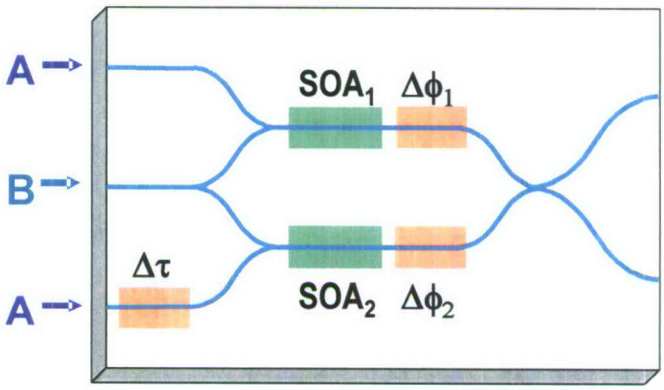

Figure 1: Schematic drawing of a unit cell that represents the heart of the photonic integrated circuit under investigation. A and B are to represent different wavelengths of input signals. Four amplifiers are shown; two are used to bias the two arms of the interferometer (SOA_1 and SOA_2), and two are for adding a phase shift to the propagating signals ($\Delta\Phi_1$, $\Delta\Phi_2$). (A time delay element, $\Delta\tau$, is also illustrated, but was not investigated here.)

There are a number of different approaches to integrating active devices, such as lasers and SOAs, with passive components, such as waveguides and MMI couplers, each having distinct advantages and disadvantages. The twin waveguide technique was first proposed and demonstrated by Suematsu, *et al.* [1]. The design vertically integrates an active and passive waveguide together allowing optical mode transfer between them. The entire structure can be grown epitaxially as a single heterostructure and the devices can be fabricated using standard fabrication techniques. Later work by Campbell and Bellavance [2] expanded and improved upon the design. A key feature common to all of the twin-waveguide designs is that the lower passive level has a higher bandgap, ensuring that the passive waveguide is transparent to the

propagating light and absorption will be minimized. In these earlier designs, the power transfer between the active and passive structures occurs via evanescent coupling where the radiation leaking from the active region excites modes in the passive waveguide [2]. The structures were symmetric designs in that both the even and odd modes have equal confinement factors in each of the two layers [3], where the effective indices of the two layers are the same [4]. Therefore, precise control over the composition and thickness of the epitaxial layers was necessary. Additionally, the two layers need to be close to each other to maximize the overlap of the evanescent fields leaking from one waveguide to the other.

To address many of the problems inherent to the symmetric twin-waveguide design, Studenkov, *et al.* [4-8] developed the asymmetric twin-waveguide (ATG). The asymmetry refers to the differing effective indices between the active and passive layers. Therefore, the even and odd mode will encounter different refractive indices, propagate differently, and will not couple with each other. In this design, the even mode is concentrated in the active region and the odd in the passive region. With electrical pumping, the active region will have gain and the even mode will dominate in the twin-waveguide region. In order to couple between the active and passive waveguides, an adiabatic taper is used [4]. By slowly varying the width of the active waveguide along the taper, the effective index will also slowly change. At a particular width, the active and passive waveguides will be locally symmetric, have matching effective indices, and a strong local resonance will exist between the two modes. Therefore, there will be strong coupling and optical power will be transferred from one mode to the other. The end width of the taper is sufficiently small, less than 1 μm, to ensure that the taper's effective index is insignificant, to minimize any reflections, and to maximize coupling. The asymmetric twin-waveguide has been used to integrate a wide variety of devices, such as lasers, SOAs, modulators, photodetectors, and other components [9-12]. We have implemented the ATW method for the integration of the passive waveguides with the SOAs in the PIC under design, fabrication and characterization.

The Beam propagation method (BPM) was used to assist determination of an appropriate epitaxial layer design, using the software program RSoft BeamPROP (Version 5.0) for calculations. The passive waveguide ridge is configured as a dilute waveguide, embedding several layers of higher index InGaAsP within an InP waveguide [13-15]. The quaternary material chosen was $In_{0.8}Ga_{0.2}As_{0.45}P_{0.55}$ with a characteristic wavelength of 1180 nm. The whole structure was n-doped with sulfur at a concentration of $5x10^{17}$ cm^{-3}. The substrate has a nominal n-type background doping of $1\text{-}8x10^{18}$ cm^{-3} to allow for current flow to a backside contact. The dilute waveguide structure chosen has 100, 250, and 100 nm thick $In_{0.8}Ga_{0.2}As_{0.45}P_{0.55}$ quaternary layers separated by 200 nm layers of InP. The refractive indices of InP and the quaternary at 1550 nm are 3.167 and 3.29, respectively, yielding an effective index of 3.22 using the weighted squares method. The design was optimized for a ridge waveguide that is 4 μm wide and 1.05 μm tall. The active portion of the epitaxial structure was a double heterostructure configuration. The active region was centered about a 200 nm thick $In_{0.56}Ga_{0.44}As_{0.94}P_{0.06}$ quaternary layer emitting at 1550 nm in order to amplify the incident data pulse. The active region was surrounded by 100 nm of the same 1180 nm quaternary material that was used in the passive waveguide. There was no doping in the active region. The cap layers consisted of InP, with highly-doped 1180 nm and 1550 nm InGaAsP serving as contact layers for the p-type metallization. The spacing between the active region and the cap was simulated using BPM and chosen to be 700 nm [16] to reduce mode overlap with the highly-doped cap layer. The spacer thickness was chosen as 200 nm to

maximize power transfer. A number of sacrificial etch stop layers were placed throughout the device to assist fabrication. The epitaxial structure, shown schematically in Figure 2 and grown using metalorganic chemical vapor deposition (MOCVD), was purchased from IQE, Inc.

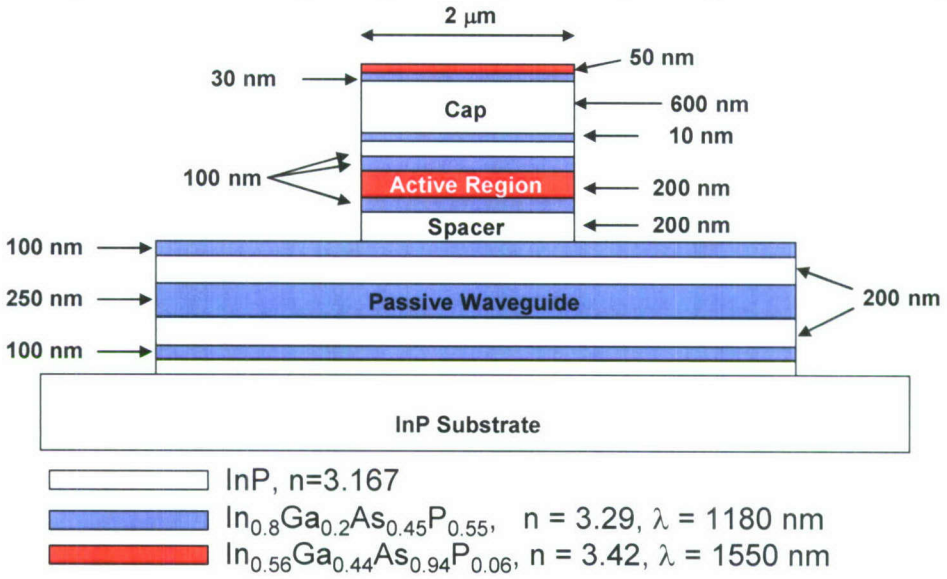

Figure 2: Schematic of the epitaxial heterostructure designed for the asymmetric twin waveguide passive/active coupling scheme [designed with RSoft BeamProp (Version 5)].

Figure 3 shows a schematic diagram of the asymmetric twin waveguide coupling scheme designed to integrate the passive and active regions of the PIC. The taper length was chosen to be 175 μm, with optical power transfer at that length modeled to be approximately 96%. Multimode interferometers were simulated and designed for 1x2 and 2x2 configurations. Their height corresponds to the 1.05 μm height of the passive ridge waveguide. The 4 μm wide input and output waveguides were separated by a 2 μm trench. Using guided-mode propagation analysis and BPM simulations at 1550 nm, the optimized dimensions for the 1x2 MMI were determined to be 159 μm long and 12 μm wide. The optimum 2x2 MMI dimensions were determined to be 480 μm long and 18 μm wide.

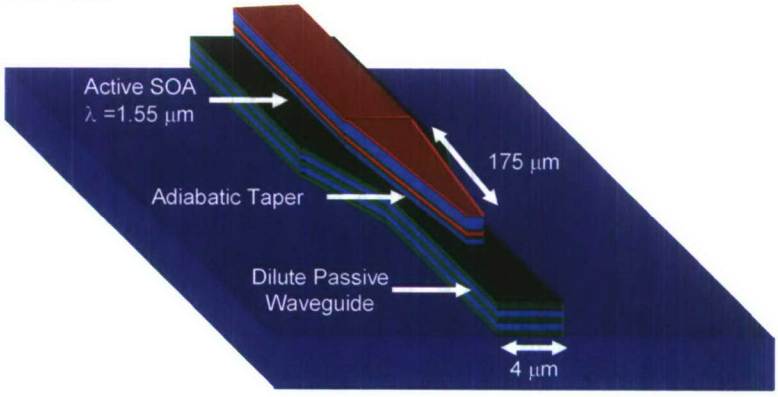

Figure 3: Schematic diagram of the asymmetric twin waveguide showing coupling between dilute passive waveguide and the active SOA region using the 175 micron-long adiabatic taper.

The vertical integration scheme complicates the fabrication process because the device must be processed on two levels, one layer containing the active devices and the other layer containing the passive structures, in addition to its two-dimensional planar layout. All of the passive waveguide interconnects, including the SOA regions, were placed within a 36 μm wide trench, a distance picked to be well outside the lateral evanescent coupling range of the waveguides. The trench design significantly reduced the etch load of the reactive ion etch (RIE) tool by not requiring etching of the broad regions between waveguides. This simple design change reduced the volume of semiconductor material etched by 91%, resulting in improvements to the etch anisotropy, a slight increase in etch rate, and less occurrence of re-deposition and micro-masking during the dry etching.

Quarter wafer segments of 2" InP wafers were fabricated with nine die per quarter. Each die contained both integrated MZI structures and discrete devices for characterization, with waveguide inputs and outputs placed on a 250 μm pitch to allow for coupling to ribbon fiber. Fabrication began with the definition of the active ridge using an AZ-5214 image-reversal resist photolithography to liftoff e-beam evaporated Ti/Pt (20/20 nm). A 450 nm SiO_2 hardmask was deposited using plasma-enhanced chemical vapor deposition (PECVD) and then photolithographically-patterned before dry etching in a CF_4 chemistry. The oxide hardmask defined the adiabatic tapers, active ridge and trench, overlapping the Ti/Pt metal to form a dual mask, with the Ti/Pt intended as part of an ohmic contact to the InGaAs surface. The resist was stripped and the semiconductor material forming the active ridge and tapers was dry etched using an inductively coupled plasma reactive ion etcher (ICP-RIE) to a depth of about 1.39 μm.

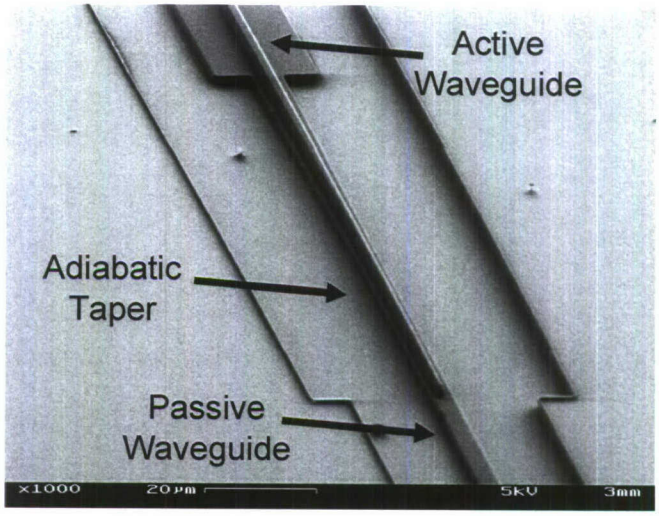

Figure 4: Scanning electron microscope image of the twin of the fabricated twin waveguide structure etched in the InP/InGaAsP semiconductor material.

After the first semiconductor etch, the now-defined active ridge required protection from subsequent processing damage, particularly the reactive ion etch (RIE) of the passive ridge. In addition to any oxide hardmask remaining from the first etch, another 450 nm PECVD SiO_2 layer was deposited over the whole wafer, which conformally-coated the exposed top and side surfaces of the active ridge. A photolithographic step using AZ-5214 as a positive tone resist defined the passive waveguides, including the MMIs. This pattern was transferred to the oxide

hardmask using the same CF_4 RIE process and the 1.04 μm deep passive ridge was etched in the semiconductor material using ICP-RIE. All oxide material was stripped in a wet buffered-oxide etch (BOE) leaving the asymmetric twin waveguide structure etched in the InP/InGaAsP material (Figure 4). Unfortunately, the BOE's fluorine chemistry also unintentionally removed the Ti/Pt metal, which had protected the sensitive ohmic contact surface through the aggressive physical bombardment of the dry etch processes.

Before depositing contact metallization, a spin-on dielectric, benzocyclobutene (BCB), was deposited as a planarization layer using the manufacturer's recommended recipe. An additional benefit of the trench geometry was that the trenches trap the planarization liquid during the spin application, completely filling the trenches and providing excellent planarization. RIE using a CF_4/O_2 plasma was used to etch back the BCB and reveal the top surface of the active ridge for metallization. The ratio of gases is important to the etch rate and etch characteristics [16, 17] and a 60% CF_4 mixture was used. By etching in short steps with frequent visual inspection, etching was terminated just as the top surface of the ridge was exposed. Next, a liftoff procedure was used to define e-beam evaporated Ti/Pt/Au (30/20/200 nm) metal contacts to the p-type material. A cross-sectional scanning electron micrograph is seen in Figure 5 of the planarized and metalized device.

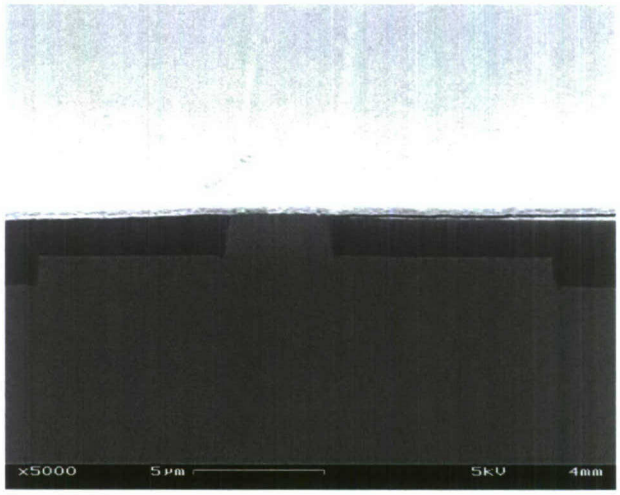

Figure 5: Cross-sectional scanning electron microscope image of the fully-fabricated asymmetric twin waveguide SOA showing the dual ridges, the benzocyclobutene (BCB) planarization layer and the Ti/Pt/Au ohmic contact. The top active ridge is 4 μm wide.

Backside processing included lapping the wafer using a 5 μm Al_2O_3 powder to thin the wafer from a starting thickness of 350 μm to approximately 150-175 μm. A 1% bromine-in-methanol solution was used to chemically polish the wafer backside and remove damage from the lapping procedure. A Ni/Au/Ge/Au (30/60/30/200 nm) backside n-type contact was sputtered on the surface before a rapid-thermal anneal at 450°C for 30 sec was used to alloy both the top and backside contacts. The backside of the samples was then sputter-coated with Ti/Pt/Au (50/70/50 nm), cleaved, and mounted with indium solder to a copper mount coated with Ti/Pt/Au (50/70/50 nm). A plan-view optical microscope composite image of the completed photonic integrated circuit is shown in Figure 6.

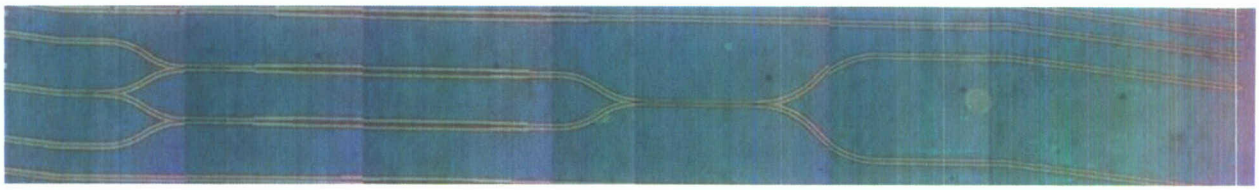

Figure 6: Composite optical microscope image (plan-view) showing 3 separate waveguide inputs, MZI, and two separate waveguide outputs. The ATG coupling scheme was used to integrate the passive and active components.

The photonic integrated circuit was composed of a number of devices including straight passive waveguides, MMI power splitters and combiners, MZI with SOAs in the arms, as well as the full unit cell seen in the schematic of Figure 1. Optical characterization was carried out on the passive components as well as the PIC. Individual SOAs were electrically biased during the propagation of optical signals to assess the degree of active/passive coupling and the amount of amplification that was provided by the SOAs. Power splitting in the MMIs was investigated and the image shown in Figure 7 shows the result. While viewing the output of a 1x2 MMI power splitter at the facet of the photonic integrated circuit, the optical signal is seen to be split 50:50 between the two output arms. Figure 8 shows the results of loss measurements carried out on the straight passive waveguides that were composed of the dilute quaternary InGaAsP interspersed between layers of InP (see epilayer schematic in Fig. 2). The data show that the loss was very low, 0.89 dB/cm, and suggests that the fabrication of the passive waveguides was successful. In addition, some waveguides contained a varying numbers of s-bends and the loss was determined for these passive devices as well (see the table in Figure 8 associated with the data for the tabulated loss results).

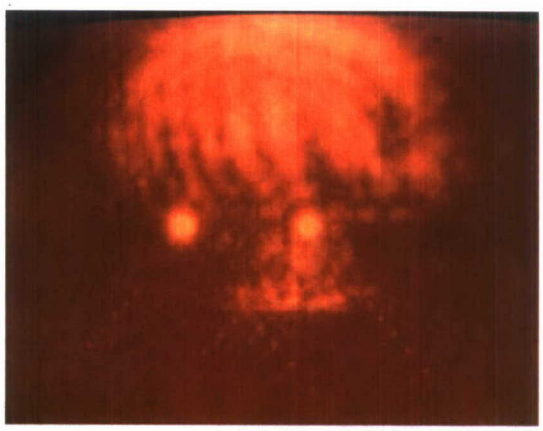

Figure 7: Light detected at the facet of the PIC showing that power is equally split between the two output arms of a 1x2 MMI device.

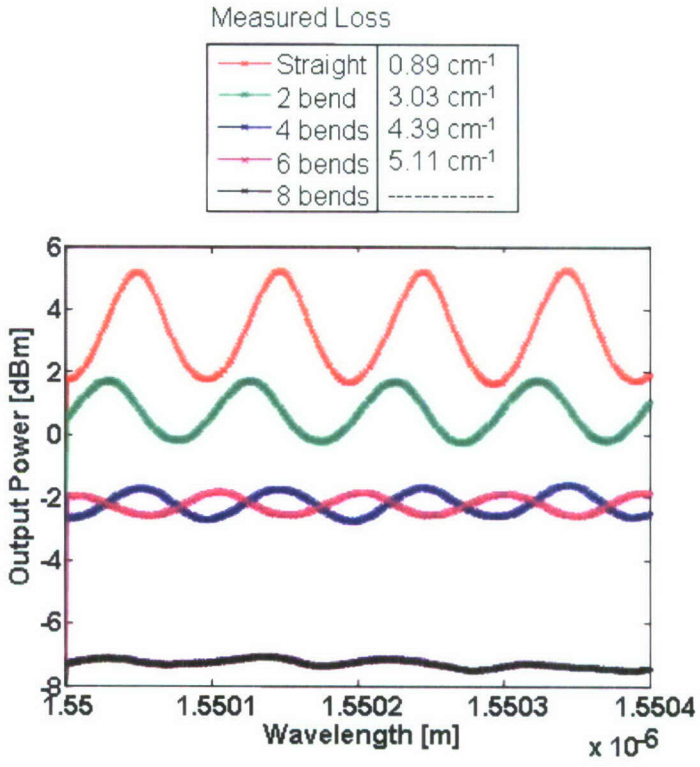

Figure 8: Loss measurements for passive waveguides with and without s-bends. The straight passive waveguides indicate a very low loss of 0.89 dB/cm suggesting etched sidewalls with a small degree of roughness.

Optical characterization was also carried out on the full MZI, with and without biasing the SOAs, to determine if the active/passive coupling scheme was successful and to determine if the SOAs were able to amplify the coupled optical signal. The optical characterization, however, indicated that issues still exist in the fabricated photonic integrated circuit. A third generation of photonic integrated circuits was required to solve the remaining fabrication issues and is currently underway. Specifically, a number of problems were found to exist. While pumping the SOAs, the I-V diode characteristics indicated that the contact resistance is larger than desired and is in the range of 10^{-4} Ω cm^2. To resolve this issue, a new epitaxial layer design, and growth, having greater doping density for the top-most semiconductor layer is necessary. Alternatively, another contact metal scheme may provide lower contact resistance. Furthermore, several SOAs were found to exhibit resistive behavior when biased. The resistive behavior is believed to be due to a problem with the BCB planarization. Occasionally, the BCB material was found to pull away from the sidewall of the SOA such that subsequent metallization would result in shorting out the SOA device. Use of BCB for the planarization layer requires further optimization. Finally, the fourth mask that was used for the metallization required re-design. Two issues were determined related to the layout of the top metal: (1) the contact pads were located too close to the top of the SOA such that SOAs were easily damaged by the electrical probe tip, and (2) the metal contact did not cover the taper resulting in significant loss to the active/passive coupling scheme. All of the issues that were identified in the optical testing of the devices and PIC have been addressed and the solutions will be implemented as Generation 3 is fabricated.

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